CLAIMS

1. (Presently Amended) An apparatus for improving stability of a magnetoresistive random access memory over process and operational variations comprising, in combination:

a current reference circuit for providing a reference current control signal;

variable analog control circuitry connected to receive the reference current control signal from the current reference circuit, where the variable analog control circuitry generates a word current reference signal in response to the reference current control signal and further generates a source current reference signal in response to the reference current control signal;

at least one word current source connected to receive the word current reference signal; and

at least one sense current source connected to receive the source current reference signal.

2. (Original) The apparatus of claim 1 further comprising in combination:

a bias tuning circuit comprising, in combination:

a bias generator having a bias output;

a plurality of switches having a word reference input and a mirror transistor output;

a plurality of mirror transistors connected to one of the mirror transistor outputs;

a transistor connected in a mirror configuration with the plurality of mirror transistors having a tuned reference output; and

a selector to select one of the mirror transistor to activate the transistor to set the voltage to the plurality of mirror transistors.

3. (Original) The apparatus of claim 2 with each one of the plurality of mirror transistors having a different gain.

4. (Original) The apparatus of claim 2 further comprising, in combination:

a pad; and

a indicator transistor in a mirror configuration with the transistor connected to the pad to provide an indicator.

5. (Original) The apparatus of claim 4 with the pad being an external pad.

6. (Original) The apparatus of claim 4 with the indicator transistor having a gain that is a multiple of the transistor.

7. (Original) The apparatus of claim 2 with the plurality of mirror transistors are n-channel transistors.

8. (Original) The apparatus of claim 2 with the plurality of switches being transistors.

9. (Original) The apparatus of claim 2 with the transistor being an N-channel transistor.

10. (Original) The apparatus of claim 2 with the bias generator being a temperature and voltage compensated bias generator.

11. (Original) The bias turning circuit of claim 2 with the selector selecting one of the plurality of mirror transistors to compenstate of a tested parameter.

12. (Original) The apparatus of claim 2 with the tested parameter being manufacturing variance.

13. (Original) The apparatus of claim 1 further comprising in combination:

a word current source comprising, in combination:

a control circuit having a control input;

an n-channel transistor including a gate, a source and a drain, where the source is coupled to a supply ground, the drain is coupled to the magnetoresistive random access memory circuit and the gate is connected to the control input; and

a positive supply voltage, coupled to the magnetoresistive random access memory circuit so as to allow current to flow through the magnetoresistive random access memory circuit when an activation signal is applied to the gate by the control circuit.

14. (Original) The apparatus of claim 1 wherein the control circuit comprises a voltage regulator that regulates a voltage level at the gate, so as to limit an amount of current flowing through the n-channel transistor and the magnetoresistive random access memory circuit.

15. (Original) The apparatus of claim 14 with the voltage regulator comprising a feed back amplifier.

16. (Original) The apparatus of claim 14 with the voltage regulator being current controlled.

17. (Original) The apparatus of claim 13 with the n-channel transistor comprising a complementary metal oxide semiconductor n-channel field effect transistor.

18. (Original) The apparatus of claim 17 wherein the control circuit comprises a current regulator that regulates current flowing through the complementary metal oxide semiconductor (CMOS) n-channel field effect transistor when the CMOS n-channel field effect transistor is turned on and off.

19. (Original) The apparatus of claim 13 with the control circuit comprising a stabilization amplifier.

20. (Original) The apparatus of claim 19 with the stabilization amplifier further comprising, in combination:

a logic control having a read/write input, an on/off input, a write reference gate control signal and a read reference gate control signal;

a read reference switch having a read reference input and a reference output, with the read reference switch having a read reference control connected to the read reference gate control signal;

a write reference switch having a write reference input and a write reference output connected to the reference output, with the write reference switch having a write reference control connected to the write reference gate control signal; and

a feedback amplifier connected to the reference output, having a mirror current output and a mirror feedback voltage input.

21. (Original) The apparatus of claim 13 with the control input being a regulated mirror gate signal.

22. (Original) The apparatus of claim 1 with the sense source further comprising, in combination:

a reference transistor having a gate, a current reference input and a voltage supply input; and

a plurality of transistors in a mirror configuration with the reference transistor with each gate of the plurality of transistors connected to the gate, with the plurality of transistors each providing a sense current.

23. (Original) The current controlled current source of claim 22 with the plurality of transistors being P-channel transistors.